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DATE: Monday, June 27, 2005

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L10: Entry 2 of 2 File: USPT Jul 13, 1993

DOCUMENT-IDENTIFIER: US 5228139 A
** See image for Certificate of Correction **
TITLE: Semiconductor integrated circuit device with test mode for testing CPU using external signal

Application Filing Date (1):
19920221

Detailed Description Text (10):
When the selecting circuit 25, to which above-mentioned signals are supplied, is being specified a test operation by a mode signal MODE is supplied from outside, if an address signal corresponding to the register Ra is supplied from outside and at the same time a read operation is specified by a read/write signal, the selecting circuit 25 asserts a selecting control signal .phi.ar and controls the output gate 20 to be in an ON state to make an interruption signal INT12 readable at the outside. In this case, if write operation is specified by a read/write signal the selecting circuit 25 asserts a selecting control signal .phi.aw to be given to a control terminal of the flip-flop circuit 21 to make a test signal TEST12 be latched by the flip-flop circuit 21.

Detailed Description Text (11):
When a fixed test operation is being specified by a mode signal MODE supplied from outside, if an address signal corresponding to the register Rb is supplied from outside and at the same time write operation is specified by a read/write signal a selecting control signal .phi.bw to be given to a control terminal of the flip-flop circuit 23 is asserted and a switchover control signal CONT12 is latched by the flip-flop circuit 23. When the switchover control signal CONT12 is in a high level, the multiplexer 22 selects an interruption signal INT12 and when the signal CONT12 is in a low level a latch signal of the flip-flop 21 is selected. In this case, if read operation is specified by a read/write signal, a selecting control signal .phi.br is asserted and a latch signal of the flip-flop circuit 23 is read out and it is output through the readout gate 24 to the data bus DB. A latch signal of the flip-flop circuit 23 takes a low level to be initialized by the reset signal RESET in response to initializing reset of the single-chip microcomputer 10.

Detailed Description Text (17):
When a mode signal MODE is 0 the mode is in the test mode and when it is 1 the mode is in the normal operation mode. In the normal operation mode a flip-flop circuit 234 in the register Rb2 is reset by a MODE signal, so that the AND gate AG 2 is controlled to be in a nonconducting state; therefore the output of the register Ra2 comprising flip-flop circuits 211, 212 and 213 is not delivered to the CPU. In the normal operation mode, the register Rb1, comprising flip-flop circuits 231, 232 and 233, is used for allowing or prohibiting the transmission of interruption signals INT121, INT122, INT123 to the CPU 11 by controlling the AND gate AG 1. Output gates 201, 202 and 203 in the register Ra1 are used in the normal operation mode for monitoring the condition of an interruption signal. In the test mode, if 1 is written in a flip-flop circuit 234 in the register Rb2, the AND gate AG 2 is controlled to be in a conducting state, so that the output of the register Ra2, comprising flip-flop circuits 211, 212 and 213, can be input to the CPU. In this

time, for the register Rb1, comprising flip-flop circuits 231, 232 and 233, if nothing is written, flip-flop circuits 231, 232 and 233 are reset, so that interruption signals INT121, INT122 and INT123 are not delivered to the CPU. In the normal operation mode, a write signal .phi.a2w for the register Ra2, and a write signal .phi.b2w for the resister Rb2 do not reach an operating level, so that the addresses of Ra2 and Rb2, address 2 and address 3, can be used for other purposes in the normal operation mode.

CLAIMS:

18. A single-chip microcomputer having a test mode and a normal operating mode, the single-chip microcomputer being in the test mode when receiving a test mode signal, the single-chip microcomputer comprising:

an internal bus including an address bus, a data bus and a control bus;

a central processing unit coupled to the internal bus and having an input;

a function module which is coupled to the internal bus and which selectively supplies an interrupt signal;

external terminals;

an input circuit coupled between the external terminals and the internal bus;

a multiplexer having an output coupled to the input of the central processing unit, a first input coupled to receive the interrupt signal, a second input coupled to receive a test interrupt signal and a control input coupled to receive control data, the multiplexer being responsive to the control data and generating the test interrupt signal on the second input thereof at the output thereof instead of the interrupt signal on the first input thereof;

a first register including a first flip-flop circuit having an input coupled to the data bus, an output coupled to the second input of the multiplexer and a control terminal coupled to receive a first select signal, the first flip-flop circuit being responsive to the first select signal and latching the test interrupt signal supplied from at least one of the external terminals to the data bus via the input circuit in the test mode;

a second register including a second flip-flop circuit having an input coupled to the data bus, an output coupled to the control terminal of the multiplexer and a control terminal coupled to receive a second select signal, the second flip-flop circuit being responsive to the second select signal and latching the control data supplied from at least one of the external terminals to the data bus via the input circuit in the test mode;

selector means coupled to the address bus and to the control bus and responsive to the mode control signal, an address signal on the address bus and a control signal on the control bus and for generating the first or second select signal to the control terminal of the first or second flip-flop circuit which is designated by the address signal,

whereby an interrupt sequence of the central processing unit is tested without generating the interrupt signal from the function module.

19. A single-chip microcomputer according to claim 18, further comprising:

an output circuit coupled between the external terminal and the internal bus,

wherein the first register further includes a gate circuit coupled to receive a

third select signal from the selector means and responsive to the third select signal and for outputting the interrupt signal to at least one of the external terminals via the data bus and the output circuit, thereby testing an operation of the function module.

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L7: Entry 3 of 16 File: USPT Jul 18, 1989

DOCUMENT-IDENTIFIER: US 4849702 A
TITLE: Test period generator for automatic test equipment

Application Filing Date (1):
19881208

Detailed Description Text (9):
A flip-flop 74 enables either the first or the second timing interval generator to define the initial test period and to thereafter alternate between the two timing interval generators. Flip-flop 74 generates signal AEN at its non-inverting (Q) output terminal and supplies AEN to the D input terminal of flip-flop 54. The first timing interval generator 30 is enabled to receive a triggering input signal when signal AEN is logic low. Flip-flop 74 generates signal BEN at its inverting output terminal and supplies BEN to the D input terminal of flip-flop 64. The second timing interval generator 40 is enabled to receive a triggering input signal when signal BEN is logic low. Signal ATZ is coupled to the set input terminal of flip-flop 74, while signal BTZ is coupled to the reset input terminal of flip-flop 74.

Detailed Description Text (12):
After a predetermined time interval has passed subsequent to the beginning of the first phase test period, a second phase test period is begun. The duration of this predetermined time interval is determined by the data loaded into counter 34 and vernier 36 from the central processing unit. When the first clock signal ACK restarts, counter 34 starts counting clock pulses. After a preselected number of clock pulses have been counted, counter 34 supplies a signal to the delay-line vernier 36. Vernier 36 delays this signal by an amount equal to a preselected delay, and then switches the first transfer signal, ATS, to logic high. The positive edge of signal ATS propagates through OR gate 52 and into the clock terminal of flip-flop 64. Flip-flop 64 switches signal BGT to the logic low state, which in turn causes the second clock signal, BCK, to stop. The second time zero signal, BTZ, goes positive a short time later, after propagating through delay line 66 and buffer 68. The positive edge of BTZ designates the beginning of the second phase test period. The positive edge of signal BTZ loads data into counter 44 and vernier 46, resets transfer signal BTS to logic low, and activates the reset input terminal of flip-flop 74. Flip-flop responds by setting signal AEN to logic low and signal BEN to logic high. The positive edge of signal BTZ also causes a positive edge in signal TZ.

Detailed Description Text (24):
A flip-flop 152 enables either the first or the second timing interval generator, 110 or 120, to define the initial minor test period and to thereafter alternate between the two timing interval generators. The non-inverting (Q) output terminal of flip-flop 152 is connected to the D output terminal of flip-flop 134. The inverting output terminal of flip-flop 152 is connected to the D input terminal of flip-flop 144. Signal MNATZ is coupled to the set input terminal of flip-flop 152, while signal MNBTZ is coupled to the reset input terminal of flip-flop 152. When the non-inverting output terminal of flip-flop 152 is at a logic low state, the first timing interval generator 110 is enabled to receive a triggering input signal. Conversely, when the inverting output terminal of flip-flop 152 is at a

logic low state, the second timing interval generator 120 is enabled to receive a triggering input signal.

Detailed Description Text (30):
A flip-flop 202 enables either the first or the second timing interval generator, 160 or 170, to define the initial free-run test period and to thereafter alternate between the two timing interval generators when the timing subsystem is in external sync mode. The non-inverting (Q) output terminal of flip-flop 202 is connected to the D input terminal of flip-flop 184. The inverting output terminal of flip-flop 202 is connected to the D input terminal of flip-flop 194. Signal FRATZ is supplied to the set input terminal of flip-flop 202. Signal FRBTZ is supplied to an input terminal of OR gate 178. The output terminal of OR gate 178 is connected to the reset input terminal of flip-flop 202. When the non-inverting output terminal of flip-flop 202 is at a logic low state, the first timing interval generator 160 is enabled to receive a triggering input signal. Conversely, when the inverting output terminal of flip-flop 202 is at a logic low state, the second timing interval generator 170 is enabled to receive a triggering input signal.

Detailed Description Text (35):
FIG. 7 illustrates the circuitry of the reference driver trigger delay circuit 27. Two parallel channels 250 and 252 are provided, one for the generation of a rising edge delay signal, RED, and the other for the generation of a falling edge delay signal, FED. The rising edge channel 250 includes a delay counter 254, a high-resolution vernier 256, a delay memory 258, and a delay program step counter 260. Clock signal CK is applied to a clock input terminal of counter 254, while time-zero signal TZ is applied to load input terminals of both counter 254 and vernier 256. An input terminal of vernier 256 is connected to an output terminal of counter 254. An output terminal of vernier 256 generates the rising edge delay signal RED. Delay memory 258 is coupled to both counter 254 and vernier 256 for supplying data to define the duration of the delay through channel 250. The delay memory receives the data from the central processing unit 28. It contains a plurality of entries, with each entry defining a separate delay time. Counter 260 serves as an address pointer to indicate which entry in the delay memory is to be loaded into the counter and vernier. Counter 260 has the capability of incrementing its address pointer by one address upon each timing cycle. A trigger delay mode register 262 is coupled to counter 260 for selecting its mode of operation.

Detailed Description Text (36):
Similarly, the falling edge channel 252 includes a delay counter 264, a high-resolution vernier 266, a delay memory 268, and a delay program step counter 270. Clock signal CK is applied to a clock input terminal of counter 264, while time-zero signal TZ is applied to load input terminals of both counter 264 and vernier 266. An input terminal of vernier 266 is connected to an output terminal of counter 264. An output terminal of vernier 266 generates the falling edge delay signal FED. Delay memory 268 is coupled to both counter 264 and vernier 266 for supplying data to define the duration of the delay through channel 252. The delay memory receives the data from the central processing unit 28. It contains a plurality of entries, with each entry defining a separate delay time. Counter 270 serves as an address pointer to indicate which entry in the delay memory is to be loaded into the counter and vernier. Counter 270 has the capability of incrementing it address pointer by one address upon each timing cycle. The trigger delay mode register 262 is also coupled to counter 270 for selecting its mode of operation.

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L6: Entry 1 of 6 File: USPT Dec 3, 1996

DOCUMENT-IDENTIFIER: US 5581698 A
TITLE: Semiconductor integrated circuit device with test mode for testing CPU using external Signal

Application Filing Date (1):
19930415

Detailed Description Text (17):
When a mode signal MODE is 0 the mode is in the test mode and when it is 1 the mode is in the normal operation mode. In the normal operation mode a flip-flop circuit 234 in the register Rb2 is reset by a MODE signal, so that the AND gate AG 2 is controlled to be in a nonconducting state; therefore the output of the register Ra2 comprising flip-flop circuits 211, 212 and 213 is not delivered to the CPU. In the normal operation mode, the register Rb1, comprising flip-flop circuits 231, 232 and 233, is used for allowing or prohibiting the transmission of interruption signals INT121, INT122, INT123 to the CPU side by controlling the AND gate AG 1. Output gates 201, 202 and 203 in the register Ra1 are used in the normal operation mode for monitoring the condition of an interruption signal. In the test mode, if 1 is written in a flip-flop circuit 234 in the register Rb2, the AND gate AG 2 is controlled to be in a conducting state, so that the output of the register Ra2, comprising flip-flop circuits 211, 212 and 213, can be input to the CPU. In this time, for the register Rb1, comprising flip-flop circuits 231, 232 and 233, if nothing is written, flip-flop circuits 231, 232 and 233 are reset, so that interruption signals INT121, INT122 and INT123 are not delivered to the CPU. In the normal operation mode, a write signal .phi.a2w for the register Ra2, and a write signal .phi.b2w for the resister Rb2 do not reach an operating level, so that the addresses of Ra2 and Rb2, address 2 and address 3, can be used for other purposes in the normal operation mode.

CLAIMS:

1. A method for testing an operation of a semiconductor integrated circuit device which includes a central processing unit and a functional module, the semiconductor integrated circuit device having a normal mode and a test mode, the functional module selectively generating at its output thereof a first interrupt signal to be supplied, in the normal mode, to an input of the central processing unit, through the signal separating circuit in the semiconductor integrated circuit device, wherein the signal separating circuit operating in the normal mode couples the output of the functional module to the input of the central processing unit, the method for testing comprising the steps of:

setting an operation of the semiconductor integrated circuit device into the test mode;

in response to the setting of the test mode, operatively uncoupling the output of the functional module from the input of the central processing unit through the signal separating circuit;

in the test mode, operatively coupling the signal separating circuit to the input

of the central processing unit and to an internal bus in the semiconductor integrated circuit device in response to a first control signal provided from a control signal forming circuit in the semiconductor integrated circuit device;

inputting a test signal serving as a test interrupt signal to an external terminal of the semiconductor integrated circuit device;

operatively connecting the external terminal to the internal bus;

supplying the test signal from the external terminal to the internal bus and in turn to the input of the central processing unit via the signal separating circuit; and

testing an operation of the central processing unit using the test signal.

12. A method of operating a semiconductor integrated circuit device which includes a central processing unit, a function module, an internal bus, an external terminal and an input and output circuit, the semiconductor integrated circuit device having a normal operation mode and a test mode, the method comprising the steps of:

setting the semiconductor integrated circuit device in the normal operation mode, and during the normal operation mode:

selectively generating an interrupt signal by the function module to supply the interrupt signal to a first input port of a multiplexer included in the semiconductor integrated circuit device, the multiplexer having a second input port and an output port where the output port is operatively connected to the central processing unit;

controlling operation of the multiplexer through operation of a first control circuit of the semiconductor integrated circuit device to operatively connect the first input port of the multiplexer to the output port of the multiplexer, so that the interrupt signal generated by the function module passes to the central processing unit through the multiplexer;

setting the semiconductor integrated circuit device in a first operation of the test mode, and during the first operation of the test mode:

controlling the operation of the multiplexer through operation of the first control circuit to operatively disconnect the first input port of the multiplexer from the output port of the multiplexer;

supplying to the external terminal an externally generated test signal serving as a test interrupt signal;

interfacing the external terminal, the input and output circuit and the internal bus;

operatively connecting a first transmission circuit of the semiconductor integrated circuit device to the internal bus and the second input port of the multiplexer through a second control circuit of the semiconductor integrated circuit device;

operatively connecting the second input port of the multiplexer to the output port of the multiplexer through operation of the first control circuit;

supplying the externally supplied test signal at the external terminal to the central processing unit, through the input and output circuit, the internal bus, the first signal transmission circuit and the multiplexer;

testing an operation of the central processing unit with the test signal;

setting the semiconductor integrated circuit device in a second operation of the test mode, and during the second operation of the test mode:

controlling the operation of the multiplexer through operation of the first control circuit to operatively disconnect the first input port of the multiplexer from the output port of the multiplexer;

operatively connecting the function module to the internal bus through a second transmission circuit of the semiconductor integrated circuit device through the second control circuit;

interfacing the internal bus, the input and output circuit and the external terminal;

generating the interrupt signal by the function module;

supplying the interrupt signal generated by the function module to the external terminal, through the second transmission circuit, the internal bus and the input and output circuit; and

testing the operation of the function module with the interrupt signal.

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L6: Entry 2 of 6 File: USPT Jan 31, 1995

DOCUMENT-IDENTIFIER: US 5386563 A
TITLE: Register substitution during exception processing

Application Filing Date (1):
19921013

Brief Summary Text (6):
It is desirable that the move between the main processing mode and the exception processing mode should be reversible in that when a return is made to the main processing mode the operation of the main processing mode will continue as if it had not been interrupted. In order to achieve such reversibility, it is necessary that the contents of the various processing registers within the CPU should be saved upon leaving the main processing mode so that they can be restored after the exception processing mode has finished its use of the registers and control is returned to the main processing mode. This is conventionally achieved by saving the contents of the registers in the main processing mode to an area of stack memory in external random access memory (RAM) upon leaving the main processing mode and then returning these contents from the area of stack memory to the registers upon returning to the main processing mode.

Detailed Description Text (2):
FIG. 1 schematically illustrates a part of a CPU 2. The CPU 2 contains an internal bus 4 by which the various portions of the CPU 2 communicate. An interrupt controller 6 is attached to the internal bus 4. The interrupt controller 6 receives external inputs nFIQ and nIRQ that are signal indicating interrupt requests applied to external pins on the CPU package.

Detailed Description Text (16):
A detailed flow diagram showing the system control implemented according to this example is provided in FIG. 4A. As described above, instruction data including a software interrupt instruction is received from the external bus and eventually transferred to the instruction decoder. This is shown at step 50 of the flow diagram. Upon receipt of the software interrupt instruction, the instruction decoder notifies the interrupt controller at step 52. In this example, exception data registers R13svc and R14svc replace registers R13 and R14 respectively at step 54. The contents of R15pc from the User32 mode are saved in the R14svc register also at step 54. The contents of the CPSR from the User32 mode are saved in the SPSRsvc at step 56 and the contents of the CPSR updated to reflect the SVC32 mode which has been entered at step 58. In particular, the five bit field indicating the processing mode is updated. If, while in the SVC32 mode, a further exception occurs (steps 62) as determined at step 60, such as an aborted memory access, then the Abt32 mode is entered from the SVC32 mode.

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L6: Entry 3 of 6 File: USPT Jul 13, 1993

DOCUMENT-IDENTIFIER: US 5228139 A
**** See image for Certificate of Correction ****
TITLE: Semiconductor integrated circuit device with test mode for testing CPU using external signal

Application Filing Date (1):
19920221

Detailed Description Text (17):
When a mode signal MODE is 0 the mode is in the test mode and when it is 1 the mode is in the normal operation mode. In the normal operation mode a flip-flop circuit 234 in the register Rb2 is reset by a MODE signal, so that the AND gate AG 2 is controlled to be in a nonconducting state; therefore the output of the register Ra2 comprising flip-flop circuits 211, 212 and 213 is not delivered to the CPU. In the normal operation mode, the register Rb1, comprising flip-flop circuits 231, 232 and 233, is used for allowing or prohibiting the transmission of interruption signals INT121, INT122, INT123 to the CPU 11 by controlling the AND gate AG 1. Output gates 201, 202 and 203 in the register Ra1 are used in the normal operation mode for monitoring the condition of an interruption signal. In the test mode, if 1 is written in a flip-flop circuit 234 in the register Rb2, the AND gate AG 2 is controlled to be in a conducting state, so that the output of the register Ra2, comprising flip-flop circuits 211, 212 and 213, can be input to the CPU. In this time, for the register Rb1, comprising flip-flop circuits 231, 232 and 233, if nothing is written, flip-flop circuits 231, 232 and 233 are reset, so that interruption signals INT121, INT122 and INT123 are not delivered to the CPU. In the normal operation mode, a write signal .phi.a2w for the register Ra2, and a write signal .phi.b2w for the resister Rb2 do not reach an operating level, so that the addresses of Ra2 and Rb2, address 2 and address 3, can be used for other purposes in the normal operation mode.

CLAIMS:

18. A single-chip microcomputer having a test mode and a normal operating mode, the single-chip microcomputer being in the test mode when receiving a test mode signal, the single-chip microcomputer comprising:

an internal bus including an address bus, a data bus and a control bus;

a central processing unit coupled to the internal bus and having an input;

a function module which is coupled to the internal bus and which selectively supplies an interrupt signal;

external terminals;

an input circuit coupled between the external terminals and the internal bus;

a multiplexer having an output coupled to the input of the central processing unit, a first input coupled to receive the interrupt signal, a second input coupled to

receive a test interrupt signal and a control input coupled to receive control data, the multiplexer being responsive to the control data and generating the test interrupt signal on the second input thereof at the output thereof instead of the interrupt signal on the first input thereof;

a first register including a first flip-flop circuit having an input coupled to the data bus, an output coupled to the second input of the multiplexer and a control terminal coupled to receive a first select signal, the first flip-flop circuit being responsive to the first select signal and latching the test interrupt signal supplied from at least one of the external terminals to the data bus via the input circuit in the test mode;

a second register including a second flip-flop circuit having an input coupled to the data bus, an output coupled to the control terminal of the multiplexer and a control terminal coupled to receive a second select signal, the second flip-flop circuit being responsive to the second select signal and latching the control data supplied from at least one of the external terminals to the data bus via the input circuit in the test mode;

selector means coupled to the address bus and to the control bus and responsive to the mode control signal, an address signal on the address bus and a control signal on the control bus and for generating the first or second select signal to the control terminal of the first or second flip-flop circuit which is designated by the address signal,

whereby an interrupt sequence of the central processing unit is tested without generating the interrupt signal from the function module.

19. A single-chip microcomputer according to claim 18; further comprising:

an output circuit coupled between the external terminal and the internal bus,

wherein the first register further includes a gate circuit coupled to receive a third select signal from the selector means and responsive to the third select signal and for outputting the interrupt signal to at least one of the external terminals via the data bus and the output circuit, thereby testing an operation of the function module.

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L6: Entry 4 of 6 File: USPT May 21, 1985

DOCUMENT-IDENTIFIER: US 4519028 A
TITLE: CPU with multi-stage mode register for defining CPU operating environment including charging its communications protocol

Application Filing Date (1):
19810217

Brief Summary Text (27):
In brief summary, this invention provides a central processing unit including an operating mode register that includes independently-conditioned stages each identifying a logical characteristic of the data processing system. The central processing unit modifies the operation in response to this mode information.

Drawing Description Text (10):
FIG. 15 is a schematic diagram showing a portion of the circuitry in the central processing unit for loading the mode register shown in FIG. 3;

Detailed Description Text (110):
With reference to FIG. 25, the signals from the address/interrupt lines AI (4:1) are received in address/interrupt buffers 86 and coupled as coded priority CP (3:0) signals to a priority comparator 200 in control logic 64. The operating priority of processor 10 that is contained in status register 71 is also coupled to priority comparator 200. If the interrupt has a higher priority than the operating priority, an INT PRI OK interrupt priority signal is asserted which couples the complement of the VEC vector signal from address/interrupt line AI (5) through an AND gate 201 as an INTVEC internal vector signal. If the VEC signal is asserted when the INT PRI OK interrupt priority signal is asserted, an EXTVEC external vector signal is asserted by AND gate 202. If the INTVEC internal vector signal is asserted, a vector generator 203 is enabled to generate an interrupt vector in response to the coded priority CP (3:0) signals.

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L6: Entry 6 of 6 File: USPT Jul 30, 1974

DOCUMENT-IDENTIFIER: US 3827029 A
TITLE: MEMORY AND PROGRAM PROTECTION SYSTEM FOR A DIGITAL COMPUTER SYSTEM

Application Filing Date (1):
19720925

Detailed Description Text (65):
The flags D8 through D11 are lockout flags whose function is to prevent the occurrence of various system operations at particular times. The system 100 includes hardware for handling normal external interrupts in response to contact closures and the like and also hardware for handling service request interrupts from external devices needing only the occasional execution of a single instruction within the system. These two types of interrupts may be respectively locked out by the setting of the respective flags D10 and D11 within the designator register.

Detailed Description Text (71):
Whenever an instruction is executed within the computer system 100, the entire instruction is transferred from the central processing unit input data bus or from the fast access registers 118 (FIG. 1) into a Z data register 808 (FIG. 8). The function and mode code bits of the instruction are transferred into an F and M (function and mode) register 810 and are then interpreted by an instruction decode logic 812. All of this is shown in greatly simplified form in FIG. 8. If the instruction is one of those which may not be executed under the memory violation protect mode of operation, the instruction decode logic 812 generates one of four output signals B, C, D, or E all of which are fed into what amounts to an OR gate 14 and through what amounts to an AND gate 16 to set the instruction violation flag in the thirteenth flag position within the designator register 802. If the privileged instruction lockout flag in the ninth position of the designator register 802 is set, the D9 signal generated by this flag enables logic equivalent to the and gate 816 to pass the signal B, C, D, or E and to allow the signal to set the thirteenth instruction violation flag within the designator register 802. If the privileged instruction lockout flag is not set, then the gate 816 blocks the passage of the signal, and all instructions are executed in the normal manner.

Detailed Description Text (76):
In the example presented in the lower half of FIG. 7, "1" data bits appear in bit positions 1 and 3 of the instruction, and hence, the data from bit positions 0 and 2 of the instruction are transferred through the gate 820 and are used to adjust the eighth and ninth flags within the designator register 802. Since the data in bit positions 0 and 2 are "1" data bits, the eighth and ninth designator register flags are set, thus initiating both the privileged instruction lockout and a memory write lockout mode of computer system operation. If "0" data bits are present in the zero and second bit positions within the instruction, then these two flags are cleared by the same instruction. In a similar manner, the external interrupt lockout and service request lockout flags in the tenth and eleventh bit positions within the designator register 802 may be set or cleared in accordance with the data in bit positions four and six of the instruction, but only when "1" data bits are present within the fifth and seventh bit positions of the instruction. Since execution of this instruction by a program could clear the memory write and

privileged instruction lockout flags and grant the program unrestricted access to the system memory, the execution of this instruction is prevented during the privileged mode of operation. For this reason, the signal D is fed into the gate 814 as has been explained. It is to be understood that when the privileged mode of operation is in effect, means not shown in FIG. 8 are effective to defeat the action of the control 818 and to prevent the signal D from altering the flags within the designator register 802.

Detailed Description Text (82):
The SST instruction may also be executed out-of-sequence in response to an external system interrupt. Just as in the case of a processor interrupt, an external interrupt causes program control to commence at a fixed core location with the execution of an out-of-sequence SST instruction. In response to such an external interrupt, the SST instruction stores away all of the system registers, sets the flags 9 and 10 within the designator register 802, and clears the ninth or privileged instruction lockout flag so as to allow the interrupt programs within the system to freely execute any instructions without causing a processor interrupt. With reference to FIG. 6, during either a processor interrupt or an external interrupt operation, the NORM-M (normal mode) signal shown in FIG. 6 is not present. Therefore all portions of the system memory may be freely accessed during either a processor or an external interrupt without any interference from the memory protect subsystem 136.

Detailed Description Text (86):
The operation of both external and service request interrupts is unaffected by the protect feature of the invention. In response to an external interrupt, an out-of-sequence SST instruction is executed which sets the interrupt lockout flags 10 and 11 within the designator register 802 and which clears the privileged instruction lockout flag in the ninth position of the designator register 802 so as to allow the interrupt routines to execute any instructions without interference from the protect subsystem. The setting of the interrupt lockout flag also defeats the NORM-M signal shown in FIG. 6 and thus disables the memory protect subsystem so that the interrupt routines may have access to any portion of the system memory. The interrupt routines may return program control to the interrupted program with the protect system in operation simply by executing an EST instruction to reverse the data transfer carried out by the SST instruction following the interrupt. Service request interrupts, which are single instruction interrupts for transferring data between an external device and core, are executed in the normal manner regardless of the status of the lockout flags 8 and 9.

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